Please amend claim 11 as follows:

Sub C1 D3

11. ~~(amended) The method of claim 9 wherein said gray scale control signal has a stepped waveform over the plurality of [ILLUMINATION] ILLUMINATE periods within one frame period [, where each step in the waveform corresponds to one ILLUMINATION period].~~

REMARKS

Objections

A. 35 U.S.C. § 132

The Examiner has objected to the amendment of January 22, 1999 under 35 U.S.C. § 132 because the amendment introduces new matter into the disclosure. The applicants disagree.

FIGs. 7 and 8 were introduced in support of, for example, independent claims 8, 14, 20 and 30 at the insistence of the Examiner to provide a depiction of each and every feature of these new claims in the figures as required under 37 C.F.R. 1.83(a). Although the applicants did not believe that such drawings were necessary to understanding and practicing the invention, the prior amendment added drawings to fulfill the § 1.83(a) requirement and expedite allowance of this patent application. The drawings, as discussed below, were prepared by the applicant's undersigned attorney using the specification of the application as his sole source of information. As such, FIGs. 7 and 8 are derived directly from the specification as filed.

1. Objection of FIG. 7

As to FIG. 7, this figure depicts the various signals that exist within the electroluminiscent (EL) cell control circuit. These signals are explicitly described in the text of the specification and the applicant's attorney merely used the words of the specification to produce the figure. Specifically, the

first (top) portion of the figure depicts a frame period being divided into a plurality of LOAD and ILLUMINATE periods as described on page 3, lines 15-17 and again on page 4, lines 12-16.

The next portion of FIG. 7 depicts a relative comparison of a data signal and a ramp control signal (analog signal) within a frame period. The use of this signal is explicitly described at page 3, line 61 to page 4, line 2 where the ramp control signal varies from "5V to -5V during the field", i.e., the ramp extends over one frame period and the storage capacitor "stores -1.5V" representing a data value. Under this situation, the transistor conducts current during 32 of the 128 ILLUMINATE periods within a frame period (i.e., approximately, 25% brightness). The last (bottom) graph of FIG. 7 depicts this current being conducted during some of the ILLUMINATE periods and not conducting during other ILLUMINATE periods. The transition from conducting to nonconducting occurs approximately at a point where the ramp signal value crosses the data signal value. Thus, the first, second, and fourth graphs explicitly depict the text of the specification that describes the operation of grayscale pixel control using an analog control signal as described with respect to the example on page 3, line 61 et seq. and elsewhere in the specification.

On page 3, lines 62-64 the specification states that the "ramp of the voltage" over a frame period can be replaced with "a step function in voltage" over a frame period. This is exactly what is depicted in the third time graph of FIG. 7, a step waveform that generally follows the slope of the ramp waveform.

Clearly, the text of the specification, as filed, supports the various graphs of FIG. 7. Consequently, FIG. 7 does not add any new matter to the specification as filed. As such, the applicant believes the objection to FIG. 7 is inappropriate and respectfully requests that the objection be withdrawn.

2. Objection of FIG. 8

Similarly to the discussion above, FIG. 8 also contains various signal graphs that depict signals for digital pixel control that were explicitly described in the specification, as filed.

Specifically, on page 4, lines 12-16, the frame time is described as being divided into a number of LOAD and ILLUMINATE periods. This period arrangement is depicted in the first (top) graph of FIG. 8.

On page 4, lines 16-19, the specification states that during the LOAD periods data is loaded into the pixel circuitry based upon the significance of each data bit, i.e., the least significant bit (LSB) is loaded during the first LOAD period, the "next most significant bit" is loaded during the second LOAD period and so on. This bit significant loading is what is depicted in the second (middle) graph of FIG. 8.

The last (bottom) graph of FIG. 8 depicts the pulsed current that is conducted during the ILLUMINATE periods with respect to the significance of each bit. As described on page 4, lines 19-30 the LSB corresponds to one current pulse, the next significant bit corresponds to two current pulses, and so on.

Clearly, FIG. 8 is merely a depiction of the content of the specification, as filed, and does not contain any new matter. Consequently, the applicant believes that the objection to FIG. 8 is inappropriate and respectfully requests that the objection be withdrawn.

3. Objection of the claims 8-12 14 and 20.

The Examiner specifically objected to claims 8, 9, 10, 11, 12, 14 and 20 as not being supported by the specification, as filed. The applicant respectfully disagrees.

The Examiner objected to claim 8, lines 13-18 as not supported by the specification as filed. This particular portion of claim 8 recites:

> "storing, during each of said LOAD periods, said data line signal within said circuit; and
>
> applying, during each of said ILLUMINATE periods, a current to said electroluminescent cell and said circuit, where said electroluminescent cell is selectively illuminated in response to said current and said stored data line."

These clauses recite <u>exactly</u> the process described in the specification at page 3, lines 58 to page 4, line 2 (analog control) and again at page 4, lines 12-22 (digital control). In each instance, a data line signal is stored on the gate of transistor 80 in the pixel circuit, e.g., -1.5V, during a LOAD period to activate the pixel. See, for example, page 3, lines 13-25. Then, as described on page 3, lines 25-31, during each ILLUMINATE period, a current selectively flows through each activated pixel. This portion of the specification recites all the limitations of the quoted clause of claim 8. As such, the specification fully supports claim 8 and the objection should be withdrawn.

As for claim 9, the Examiner states that the limitation of "said gray scale control signal has a magnitude that is less than said stored data signal" lacks support in the specification as filed. In response, claim 9 has been amended to recite "a <u>value</u>" rather than "a magnitude". The specification states on page 3, line 65 to page 4, line 2 that a -1.5V stored value (with a transistor threshold voltage of V_{th}=1V) is compared to a ramp waveform that spans 5V to -5V resulting in pixel illumination in 32 of 128 ILLUMINATION periods (25% illumination over a frame period). As such, a ramp waveform (gray scale control signal) value less than the stored value (stored data signal) allows a current to flow through the EL cell. Thus, the specification

supports the amended claim language of claim 9 and the objection of this claim, and therefore should be withdrawn.

As for claim 10, the Examiner states that the recitation of "a linear ramp waveform over the plurality of ILLUMINATION periods within one frame period" is not supported in the specification. In response, the applicant has changed the term "ILLUMINATION" to "ILLUMINATE" to conform the terminology of the claim to that of the specification. Page 3, line 66 states that during "the field" (also, recited interchangeably within the specification as a "frame time" or "frame period") the data line is "ramped linearly from 5V to -5V" and, at page 3, lines 5-17, the frame period is stated as containing ILLUMINATE periods. Thus, the ramp waveform must inherently span "a plurality of ILLUMINATE periods within one frame period" which supports the limitation recited in claim 10.

As for claim 11, the Examiner objected to the limitation of "a stepped waveform over the plurality of ILLUMINATION periods within one frame period, where each step in the waveform corresponds to one ILLUMINATION period". In response, the applicant has amended claim 11 to remove the unnecessary limitation of "where each step ... period" and has changed the term "ILLUMINATION" to "ILLUMINATE" to conform the terminology of the claim to that of the specification. The amended claim is supported on page 3, line 62-64, which states that the voltage ramp can be a "step function in voltage". As such, claim 11, as amended, is supported by the specification, as filed, and the objection to claim 11 should be withdrawn.

As for claim 12, the Examiner objected to the limitation of "a digital signal containing a plurality of bits where each bit is applied to said circuit during a plurality of consecutive LOAD periods" as not being supported by the specification. This particular limitation is recited on page 4, lines 16-24 where the data is stated as being loaded in the circuitry for the LSB and then repeating the procedure for each "subframe", i.e., each LOAD period, "up to the most significant bit". Clearly, this language

supports the noted limitation of claim 12. As such, the applicant respectfully requests the objection of claim 12 to be withdrawn.

In claims 14 and 20, the Examiner objected to the limitations "dividing said frame period into a plurality of LOAD periods and a plurality of ILLUMINATE periods, where each LOAD period is followed by an ILLUMINATE period" and "during each of said LOAD periods ... data signal stored; during each of said ILLUMINATE periods, ... electroluminescent cell" are not supported by the specification as filed. The disclosures of dividing a frame period into successive LOAD and ILLUMINATE periods, referred to in the specification as sub-frames, are numerous and reiterated throughout the specifications. See for example, page 3, lines 15-16, where a "frame time" is sub-divided into "separate LOAD periods and ILLUMINATE periods". Thus, a single frame time (period) is divided into sub-periods. Note that the LOAD and ILLUMINATE periods are both recited as plural terms indicating a plurality of each period within a frame period. On page 4, line 30-34, the specification states that the procedure is equivalent "to dividing a frame into a number of sub-frames", i.e., a plurality of LOAD and ILLUMINATE period pairs. Thus, each LOAD period is followed by an ILLUMINATE period in a subframe and the subframes are repeated within a frame period. As such, the first objected clause is clearly supported by the specification. The second objected clause recites the specific operation of the gray-scale control of the circuit. This operation is clearly recited in the example at page 3, line 64 to page 4, line 2 to support claim 14 (as discussed above with respect to claim 8) and at page 2, lines 35 to 48 to support claim 20 where the specification describes the detailed operation of loading the dual transistor circuit during a LOAD period and then activating the EL cell during an ILLUMINATE period in response to the loaded data. As such, the recited limitations of claims 14 and 20 are clearly described in the specification. Therefore, the applicant respectfully requests that the objection to these claims be withdrawn.

B. 37 C.F.R. 1.75(c) - Claims 22 - 24

The Examiner objected claims 22-24 under 37 C.F.R. 1.75(c) for depending from a canceled claim. In response the applicant has amended claim 22 to depend from claim 20. With this change, the applicant respectfully requests this objection be withdrawn.

Rejections

A. 35 U.S.C. §112 - claims 8-16, 18-20, 25, and 27-29

The Examiner has rejected claims 8-16, 18-20, 25, and 27-29 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not adequately described in the specification. This rejection is respectfully traversed.

The Examiner's rejection is based upon the reasoning stated above in objecting to the specification and claims. For the reasons stated above, the applicant believes all the objections are overcome and that the specification and drawings do not contain any new matter. As such, the claims of the application are fully supported by the specification, as filed. Therefore, the applicant respectfully requests that this rejection be withdrawn.

Conclusion

The applicant submits that all of these claims now fully satisfy the requirements of 35 U.S.C. § 112. Consequently, the applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the

claims now pending in the application, it is requested that the Examiner telephone Mr. Raymond R. Moser Jr., Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

7-21-98

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CERTIFICATE OF MAILING under 37 C.F.R. § 1.8(a)

I hereby certify that this correspondence is being deposited on July 21, 1998 with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Kathleen Fajkus
Signature

7-21-98
Date of signature